Unidirectional Narrowband Physical Layer Demonstration System

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Abstract

This paper concentrates on the physical layer of a single-carrier narrowband mobile ad-hoc network. All aspects of parameter estimation and synchronization are considered and the full transmission chain has been implemented on a software defined radio (SDR) board to provide a proof of concept. The paper shows the system performance with respect to carrier frequency offset and transmitting power. Previous investigations have shown that the detection probability of the transmitted bursts has a significant impact on the overall system performance. Therefore, different training sequences are compared to detect the bursts, i.e. a maximum length sequence (m-sequence) and a constant amplitude zero autocorrelation sequence (CAZAC-sequence). The paper discusses the results obtained from our hardware demonstration system.

Keywords

Narrowband, prototypes, physical layer

1. Introduction

Multiple services as data, voice, video, broadcast messaging, etc. are requested to be transmitted over digital communication systems. In general, demand on data rate for these services is growing continuously.

It is a major concern to have required information at the right time at the right place. Besides civil communications, these requirements also apply for disaster search and rescue (SAR) missions and tactical communications. For such applications, major interests are on mobile ad-hoc networks (MANETs) where each node may not only act as a transmitter or receiver, but also as a relay station for other nodes. With these functionalities, MANETs provide a flexible, resilient and infrastructure-less communication.

In order to increase the flexibility in MANETs, software defined radios (SDRs) can be utilised as nodes (Peacock, 2007). SDRs are a collection of hardware and software

technologies to enable reconfigurable system architectures for wireless networks and user terminals which are controlled by software.

Particularly in SAR and tactical missions, wireless networks have to cope with connectivity over long distances (Alberts et al., 2000). Therefore, narrowband systems in the VHF band are utilised.

The development process of a communication system typically consists of multiple cycles. One of the first cycles considers the design and simulation of algorithms. Algorithms and components are then initially verified via simulations. However, the effects of hardware platforms are mainly reproduced by statistical models in computer simulations. Nevertheless, the considered statistical behaviour can differ from real hardware platforms available. In order to ensure that all major effects are considered and the assumed statistical models comply with the real behaviour, in a next step the designed system should be verified on a hardware prototype.

In this paper, aspects of parameter estimation and synchronization are investigated according to the proposed adaptive narrowband physical layer in (Dehm et al., 2012). Thus, the transmission chain has been implemented on a SDR board and the results obtained are presented. The paper discusses the influence of carrier frequency offset and transmission power under consideration of two different synchronization sequences with respect to bit error rate (BER) and packet error rate (PER).

2. Related Work

Communication systems for public safety and SAR missions mainly rely on narrow channel bandwidth. For these applications, popular systems are terrestrial trunked radio (TETRA) with a bandwidth of 25 kHz and TETRAPOL having a bandwidth of 10 or 12.5 kHz. However, these systems provide only low data rates (Jondral, F. K. 2005, TETRAPOL Forum, 1999). The need of a narrowband communication system is shown by the current endeavour of the NATO to standardise a narrowband waveform (NBWF) applying a 25 kHz channel bandwidth with a maximum peak rate of 96 kbit/s.

In the context of narrowband communication, Dehm et al. presented in 2012 a transmission chain to increase further the data rates with 25 kHz channel bandwidth for SAR missions. This transmission chain applies algorithms for frame synchronization, frequency offset estimation and correction as well as channel estimation.

Related work shows that a proof of concept for the considered narrowband transmission chain (Dehm et al., 2012) is still required. Hence, this paper investigates the performance of the transmission chain on a hardware platform.

3. Reference Model

In this section, the reference transmission chain (see Dehm et al., 2012) and the considered algorithms for synchronization, frequency offset estimation/correction as well as channel estimation is described.

3.1. Transmission Chain

The considered narrowband system relies on time division multiple access (TDMA). The TDMA structure contains slots with duration T_S of 60 ms as illustrated in Figure 1. The slot duration as well as the utilised modulation and coding scheme define the maximum number of payloads bits in the physical layer service data unit (PSDU). The physical protocol data unit (PPDU) is completed with training sequences for synchronization and header information prior to the PSDU.

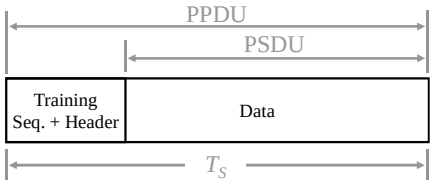

Figure 1: TDMA slot structure

Figure 2 illustrates the components of the narrowband transmission chain for transmitter and receiver operating in $B = 25\text{kHz}$ bandwidth.

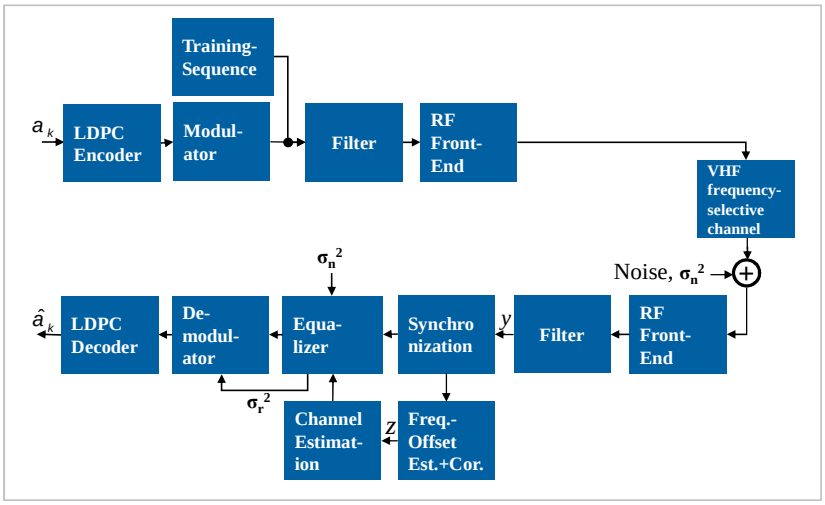

Figure 2: Narrowband physical layer transmission chain - a_k : information bit sequence, σ_n^2 : noise variance, σ_r^2 : estimated residual noise, $\hat{a}_k$: received bit sequence.

On the transmitting end, the upper layer generates a bit stream a_k which passes the irregular quasi-cyclic low-density parity-check (LDPC) encoder. Subsequently, the encoded bit stream is mapped onto symbols by the M-PSK/M-QAM modulator and a training sequence (two binary m-sequences or two complex CAZAC-sequences with equal lengths) is added. Bandwidth limitations are considered by root raised cosine (RRC) filtering prior to mixing the signal onto the carrier frequency.

The coherent receiver mixes the received signal back into the baseband domain where matched filtering is applied. Frame synchronization (detection of frames) and symbol synchronisation (determination of the position of the symbols) is achieved by exploiting the training symbols preceding the PSDU (data-aided synchronization). Additionally, the channel impulse response (CIR) is estimated using the training sequence. Based on the estimated CIR, the frequency offset between the local oscillators of transmitter and receiver is estimated and corrected. Afterwards the signal is equalized with a finite-impulse-response (FIR)-minimum mean-square error (MMSE) decision-feedback equalizer (DFE), whose coefficients are adjusted according to the estimated CIR.

For the decoding process, soft information is determined by the demodulator with respect to the equalized signal and the residual noise σ_r^2. Based on soft information, the LDPC decoder estimates the received bit stream $\hat{a}_k$.

3.2. Synchronization and Frequency Offset Estimation and Correction

One important task of receivers is to detect the beginning of data bursts (frame synchronisation). A simple method for frame synchronisation is to perform a cross-correlation of a well-known training sequence and the received signal. Once a fixed threshold is exceeded, detection of a frame is assumed. However, defining this threshold is crucial: Defining the threshold to high results in missed bursts, defining it too low, however, leads to a large number of false detections which will also cause missed or erroneous bursts since the receiver is blocked. Additionally, fading, multipath propagation, and free space loss cause a high variation of the correlation result which further impacts the synchronisation accuracy.

In communication systems, signals experience propagation delays and frequency offsets caused by oscillator instabilities and/or Doppler shifts from transmitters to the receivers. While a propagation delay can be interpreted as a constant phase shift of the data symbols, a frequency offset produces an increasing/decreasing phase shift on the signal.

In general, the propagation delay as well as the frequency offset is unknown in the receiver. To estimate the frequency offset, two consecutive m-sequences (or CAZAC-sequences) can be applied. Based on the phase shift between these two sequences, the frequency offset can be estimated.

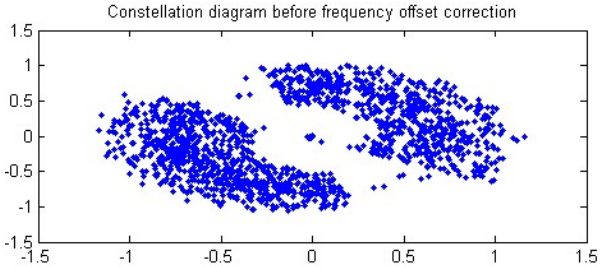

Figure 3: BPSK constellation diagram without frequency offset correction

For the estimation of the frequency offset, two cross-correlations are performed independently, each using only one of the two consecutive sequences. The vector h_1 contains *M* samples of the correlation result over the first training sequence which contains the maximum power in a predefined window. The same procedure is applied also for the second training sequence. The windowed correlation result is stored in h_2.

The frequency offset causes a continuous phase shift per symbol $\Delta\varphi$ determined by:

$$\Delta\varphi = \frac{\arg\left(h_1 \cdot h_2^H\right)}{N},$$

where *N* is the length of one training sequence.

According to the determined phase shift per symbol $\Delta\varphi$, the phase offset of the received signal y is corrected for each sample/symbol:

$$z = y \cdot e^{-j \cdot \Delta\varphi \cdot k} \quad .$$

4. Demonstration System

This section describes the SDR demonstration platform utilised to verify the algorithms and components on the hardware.

4.1. Software Defined Radio Board

The considered communication system operates in the VHF band. Analogue signals are received on a carrier frequency of $f_c = 70\text{MHz}$. The SDR-board uses an SAW (surface acoustic wave) filter to filter the received signal. After amplification using a programmable gain amplifier the signal is sampled by an analog-to-digital converter running with a sampling frequency of 92.16 MHz (sub-sampling). The SDR board is also assembled with a field-programmable gate array (FPGA). The FPGA mixes the signal into the baseband using a coordinate rotation digital computer (CORDIC) -

algorithm. Additional filtering using finite impulse response (FIR) filters as well as cascaded integrator-comb (CIC) filters is applied to reduce the sampling rate to 50 kHz which corresponds to two samples per symbol. A digital signal processor (DSP) on the SDR board processes algorithms for synchronization and frequency offset estimation.

4.2. Setup of the Demonstration System

This investigation focuses on algorithms of the coherent receiver. Hence, the transmitter is represented by a vector signal generator (VSG) (Rohde & Schwarz 1GP60, 2012). The VSG translates the modulated signal to the carrier frequency f_c and transmits it to the SDR board over a BNC cable. The BNC cable is applied to achieve reproducible results. However, wireless transmissions have also been tested applying $\lambda/2$ dipole antennas. Furthermore, a computer is connected to the SDR board via Ethernet to analyse the processed results (Wavecom Elektronik, 2010).

Figure 4 shows the schematic measurement setup and Table 1 lists the important parameters.

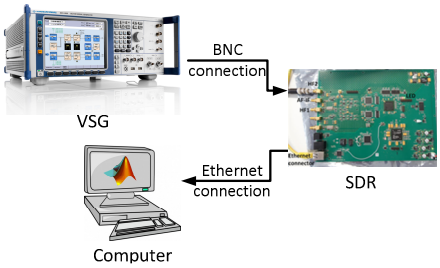

Figure 4: Schematic setup of the demonstration system

Parameter	Value
Carrier frequency (f_c)	70 MHz
Bandwidth (B)	25 kHz
TDMA slot duration (T_S)	60 ms
Length of one synchronization sequence (N)	31 symbols
Number of correlation samples (M)	7
Modulation	BPSK
Code rate	1/2

Table 1: Parameters

5. Numerical Results and Discussion

The performance of the demonstration system is investigated with respect to the packet error rate (PER) as well as the bit error rate (BER) for different carrier frequency offsets and transmit power levels. The results are compared for two types of training-sequences, binary m-sequences and complex-valued CAZAC-sequences.

5.1. Impact of Carrier Frequency Offsets on Error Rate

Local oscillators (LO) in transmitters and receivers show inaccuracies resulting in frequency offsets. Additionally, Doppler shifts contribute to frequency differences in mobile communication systems. The impact of frequency and phase offset on the constellation diagram has already been shown in Figure 3.

Frequency offset estimation and correction algorithms enable mitigation of signal distortion at the receiving end of a communication link. Remaining phase shifts can be further corrected by the equalizer, as illustrated in Figure 5.

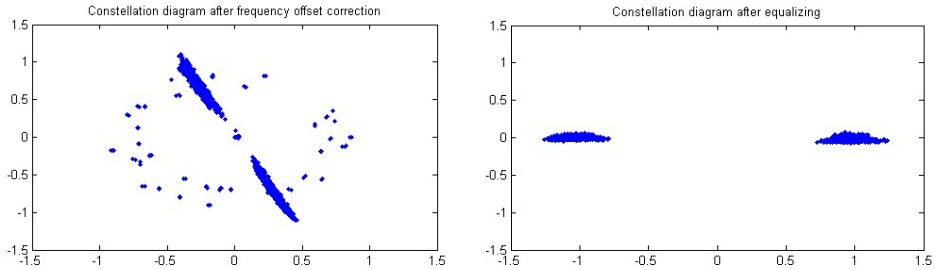

Figure 5: BPSK constellation diagram after frequency offset correction (left) and equalization (right)

In this investigation, the carrier frequency offset varies within a range of ±300 Hz. The resulting BER and PER are shown in Figure 6 for two training sequences, m- and CAZAC-sequences, respectively.

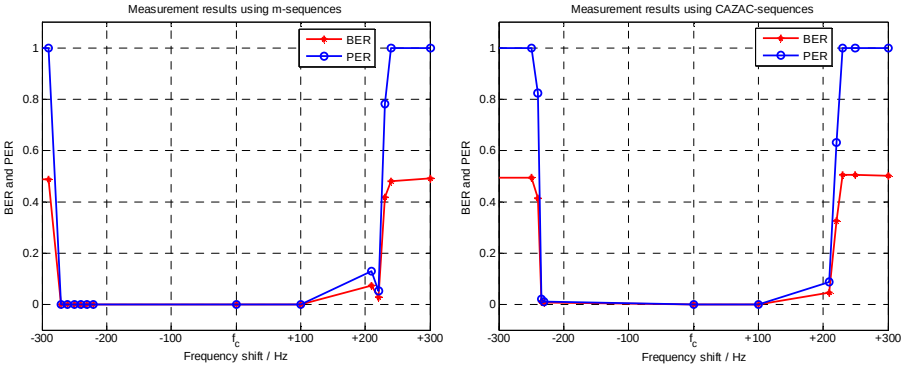

Figure 6: Carrier frequency offset versus BER/PER, left: m-sequence, right: CAZAC-sequence

The results show a strong relation between the frequency offset and the BER/PER. Both sequences provide similar performance according to the frequency offset. Although the system is designed to estimate as well as to correct frequency offsets up to ±400Hz, for both training sequences, the system achieves a low BER/PER only for frequency offsets within ±220 Hz from the carrier frequency (red and blue line). Besides this frequency operating range, the BER and PER significantly increase. A major influence on the frequency operating range has the applied frame detection algorithm. Detecting a frame according to a fixed threshold suffers from false detections resulting into high error rates in case of large frequency offsets.

According to the impact of frame detection on overall system performance, an improved synchronization algorithm with adaptive thresholds is designed and simulated.

The algorithm consists of mainly four phases:

- Phase 1: The algorithm computes the absolute value of the complex cross correlation with the synchronization sequence and the received signal.

- Phase 2: The absolute correlation results are compared to an adaptive threshold. The adaptive threshold is determined by a sliding window over the amplitudes of the received signal scaled by a predetermined factor. The first position of the correlation result exceeding the threshold is marked.

- Phase 3: From the marked position, the maximum value in a window of the length of the synchronisation sequence is determined.

- Phase 4: The detected position is verified if *N* symbols from the detected position the correlation peak from the second sequence is determined. The beginning of the information in the frame is defined according to the first detected position.

Simulations results show a gain in performance of this frame detection algorithm compared to a fixed threshold. For this synchronization algorithm, CAZAC-sequences are able to outperform m-sequences by their zero autocorrelation characteristic. In future work, this algorithm will be implemented on the SDR system and the performance of this synchronization algorithm will be investigated.

5.2. Impact of the Transmitting Power on the Error Rate

In our second measurement, the influences of different transmission power levels on the BER/PER are investigated at a carrier frequency of 70 MHz.

Figure 7 presents the degradation in the BER/PER with an increase of the transmitting power. The SNR is estimated in the receiver. As expected, SNR rises linearly according to an increase of the transmitting power. The results show that CAZAC-sequences improve the system performance slightly. A PER below 1% is reached at a transmission power of about -25.7 dBm applying CAZAC-sequences and -25 dBm applying m-sequences. The advantage of CAZAC-sequences can be explained by their good correlation properties which achieve an accurate frequency offset and CIR estimation.

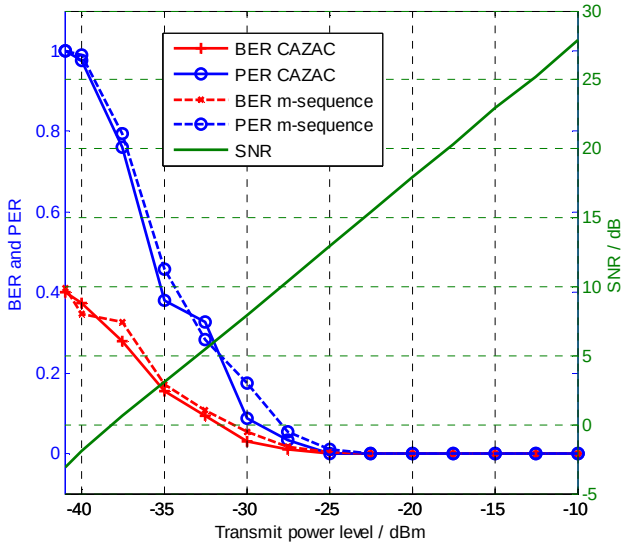

Figure 7: Transmitting power versus PER and BER

6. Conclusions

This paper has described the implementation of a narrowband transmission chain for mobile ad-hoc networks on a software defined radio platform. The impact of carrier frequency offset and transmission power on the BER and PER have been investigated. Furthermore, two types of training sequences, binary m-sequences and complex-valued CAZAC-sequences have been compared. CAZAC-sequences provide slightly better BER and PER performance compared to m-sequences. The investigation has shown that a SNR of about 7.6 dB results in a PER below 10%.

The proposed physical layer considering algorithms for symbol synchronization as well as frequency offset estimation and correction achieves also satisfactory results on a software defined radio (SDR) platform. However, the demonstration system will be further extended, e.g. with an improved frame synchronization algorithm. Thus, the demonstration system can be used for field measurements in mobile wireless scenarios.

7. References

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